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EXAMINER	
LEE, HWA C	

ART UNIT	PAPER NUMBER
2672	6

DATE MAILED: 03/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/923,233	MEI ET AL.	
	Examiner	Art Unit	
	Hwa C Lee	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) 1-6 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 7-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 14 January 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 7-20, drawn to a system for projecting processed image data onto a subject, wherein the system comprises a photolithographic process., classified in class 382, subclass 293.

   II. Claims 1-6, drawn to a method of modifying an image by rotation, classified in class 345, subclass 619.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because invention II comprises rotating an image data and extracting positional data resulting from said rotation. Said details of rotating the image data is not required for proper functioning of invention I, which discloses processing the image data but does not require the detailed limitations of rotating the image data as disclosed in claims 1-6. Invention II comprises of projecting the processed image data onto a subject, wherein the processed data is readily accessible from a memory. Said retrieval of image for projection onto a subject is independent of the image rotation and modification as disclosed by invention I. The

subcombination has separate utility such as precise rotation and other positional data required for the process is used to arrange and align the image data for projection onto a subject. Said rotation of data image does not require the system of storing and retrieving the processed image data.

3. A telephone call was made to Mr. David L. McCombs, the attorney of record on 03/02/2004 to request an oral election to the above restriction requirement but was unreachable. Subsequently, Mr. Tim Bliss returned the call on Mr. McCombs' behalf.

4. During a telephone conversation with Mr. Tim Bliss on 03/02/2004 a provisional election was made with traverse to prosecute the invention of group II, claims 7-20. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1-6 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 12 recites the limitation "a frame buffer" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claim 12 as written is dependent on claim 11, but claim 11 recites "a line buffer" and not "a frame buffer". For the purpose of art rejection, claim 12 will be considered to be dependent on claim 10 and not claim 11 as originally written.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ceglio et al., U.S. Patent No., 5,691,541 in view of Johnson et al., U.S. Patent No., 6,133,986.

4. In regards to claim 7, Ceglio et al. discloses the following:

A system for converting image data in real time, the system comprising:

a first memory operable to store the image data;

- A maskless lithography system comprises the major subsystems, which represent ***a system for converting image data*** (FIG. 5). Raw data describing mask pattern specifically is ***the image data***, which is stored in a magnetic tape (FIG. 5, No. 501), which specifically is ***a first memory operable to store the image data***. The raw data is normally compressed and is expanded into a digital image by a data preparation computer (FIG. 5, No. 502) and stored on a hard drive (FIG. 5, No. 503 and Col. 8, lines 8-11). The data preparation computer specifically is converting image data from the compressed data to a digital image (Col. 8, lines 11-18). The applicant fails to incorporate from the preamble, the limitation of converting said image data in real time into the body of the claim, and thus said limitation of converting image data in real time is not given patentable weight. However, Ceglio et al. discloses the limitation of transferring the expanded digital image into a high speed memory, such as a DRAM just before the system needs the data. Thus, Ceglio et al. discloses an on-demand transfer of the expanded digital image data, which specifically is real time conversion.

a processing device connectable to the first memory, the processing device operable to manipulate the image data;

- Said data preparation computer (FIG. 5, No. 502) specifically is ***processing device operable to manipulate the image data***. The raw

data (image data) is inputted from the magnetic tape (first memory) and is expanded into digital image data by the data preparation computer as described above.

a second memory accessible to the processing device, the second memory operable to buffer the manipulated data; and

- The expanded digital image is stored onto a hard disk (Col. 8, lines 11-18), which specifically is ***a second memory operable to buffer the manipulated data***. The data preparation computer (processing device) must access the second memory in order to store the processed data. In addition, DRAM is well known in the art to be used as a frame buffer, which specifically buffers data.

a pixel panel positioned in a first plane, the pixel panel operable to receive the buffered data and project the data upon a subject positioned in a second plane substantially parallel to the first plane

- The maskless lithography system shown in FIG. 1 represents a programmable array (FIG. 1-, No. 109) is clearly ***positioned in a first plane***. The programmable array comprises a digital micro-mirror device (DMD) (Col. 4, lines 37-64), and according to the applicant's specification, ***a pixel panel*** comprises a DMD. Thus, the programmable array specifically is ***a pixel panel***.
- The expanded digital image data, which is ***processed and buffered*** by the data preparation computer (processing device), is quickly transferred

into the programmable array. Thus the programmable array (a pixel panel) is ***operable to receive the buffered data***. Then the buffered data is projected onto substrate (FIG. 1, No. 511), which specifically is ***a subject*** (Col. 8, lines 15-28). The substrate (subject) is clearly positioned on ***a second plane substantially parallel to the first plane*** (FIG. 1, No. 511). Ceglio et al. does not specifically disclose the limitation of the pixel panel located on a first plane ***positioned at an angle relative to the subject***. However, the applicant does not specify the angle, and thus FIG. 1 satisfies the limitation of an angle as disclosed herein. In addition, a computer control system (FIG. 5, No. 506) is connected to stage metrology system (FIG. 5, No. 509), which drives scanning stage (FIG. 5, No. 510), which moves the substrate (subject). Thus, when the subject is moved, the programmable array (pixel panel) will be positioned at a plurality of angles relative to the subject.

5. In addition, Johnson clearly discloses the limitation of the pixel panel plane ***positioned at an angle relative to the subject*** (Col. 5, lines 21-39 and FIGS. 4-6).

6. It would have been obvious to one or ordinary skill in the art to take the teachings of Ceglio et al. and to add from Johnson the method of rotating the pixel panel plane at an angle relative to the subject in order to maximize the amount of images printed on the subject. By rotating the pixel panel, which projects the image, the images can be projected on maximum surface area of the subject substrate, and thus maximize the

usage of the subject substrate for printing fabricating semiconductor wafers. In addition, both references are directed, at least in part, to processing and converting image data.

7. In regards to claim 13, Ceglio et al. discloses the limitation of expanding (decompressing) compressed data into digital image by a data preparation computer for storing the manipulated data onto a hard drive as applied to claim 7 above. The data preparation computer is specifically a processor, and since the manipulated data is in a digital form, the processor must be ***a digital signal processor***. In addition, for the data preparation computer to store the digital image data onto a hard drive, a digital signal processing must be performed.

8. Claims 8, 14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ceglio et al. in view of Johnson as applied to claims 7 and 13 above, and further in view of Matsuo et al., U.S. Patent No., 5,448,689.

9. In regards to claim 8, Ceglio et al. and Matsuo et al. in combination disclose the following:

The system of claim7 wherein the processing device includes a plurality of instruction operable to calculate an address so that the image data is correctly displayed on the pixel panel.

- Ceglio et al. discloses that a small section of a programmable array (FIG. 2, No. 200), which comprises DMD devices, is shown to consist of a plurality of individual addressable mirror elements (FIG. 2, No. 201) arranged in an array (Col. 5, lines 48-52). The computer control system orchestrates the proper image transfer to the programmable array (pixel

panel) as applied to claim 1 above. While Ceglio et al. does not explicitly disclose the limitation of calculating an address, in order to properly transfer the image to the programmable array, which results in proper display of the image on said programmable array, the computer control system must calculate an address for each addressable mirror device. In addition, Ceglio et al. stresses the need for high-speed transfer of the image data onto the programmable array, the address for each addressable mirror device must be calculated quickly. Such quick calculation must be performed by a plurality of computer instructions in parallel in order to calculate the required address for each addressable mirror device.

- Matsuo et al. discloses a system for a high-speed processing and converting graphics data (Col. 2, lines 19-27). In addition, Matsuo et al. clearly recites the limitation of calculating an address for proper display of image data (Col. 5, lines 57-66). Further, Matsuo et al. discloses a system memory, wherein instructions, commands, data, and programs, etc. processed by the CPU is stored (Col. 5, lines 16-53). Said instructions are a plurality of instructions processed by the CPU for operating the system, which comprises calculating the address.

10. It would have been obvious to one of ordinary skill in the art to take the teachings of Ceglio et al. and Johnson, and to add from Matsuo et al. the method of calculating an address in order to properly display the image data on the pixel panel. The teachings

by Ceglio et al. and Johnson comprise a processor for converting an image data and transferring the converted data onto a display unit (programmable array). Matsuo et al. improves upon the image processor of Ceglio et al. by calculating both the physical address of the display memory and the logical address of the drawing location, which allows for accurate location of the desired image data from memory and accurate display location on the display unit. In addition, all references are directed, at least in part, to processing and converting image data.

11. In regards to claim 14, the same basis and rationale for claim rejection as applied to claims 7 and 8 are applied.

- As applied to claim 7 above, processing the image data stored in a magnetic tape (first memory); storing the manipulated image data onto a hard drive (second memory); and transferring the manipulated image onto the pixel panel to be displayed are specifically ***retrieving at least a portion of the image from a memory***.
- As applied to claim 8 above, Matsuo et al. clearly discloses calculating both the physical location of the image data in memory and the drawing location on the display, which specifically is ***calculating at least one address for the image portion, the calculation operable to determine the position of the image portion on a pixel panel positioned in a first plane***. In addition, the limitation of the first plane ***rotated relative to the subject*** is specifically having the first plane at an angle relative to the subject as applied to claim 7 above. Ceglio et al. also discloses the

limitation of ***the subject positioned in a second plane that is substantially parallel to the first plane*** as applied to claim 7 above.

- As applied to claim 7 above, Ceglio et al. discloses a second memory comprising a DRAM, and it is well known in the art that a frame buffer is built generally using a DRAM or a VRAM. Thus, transferring the manipulated digital image data onto a DRAM is specifically ***transferring the image portion to a buffer***, and transferring the stored manipulated digital image data onto the programmable array is specifically ***transferring the image portion from the buffer to the pixel panel.***

12. In regards to claim 16, the same basis and rationale for claim rejection as applied to claims 7-8 and 14 are applied. The rotation of the pixel panel plane relative to the subject plane must be used to calculate the image portion location in order to project the image data on the desired area of the subject.

13. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ceglio et al. in view of Johnson as applied to claims 7 and 13 above, and further in view of Morooka, U.S. Patent No., 5,200,925.

14. In regards to claim 9, Ceglio et al. and Johanson in combination disclose the limitations of claim 7 as applied above, wherein processed (manipulated) image data is transferred and stored onto a second memory comprises any high-speed memory such as DRAM, but do not explicitly disclose the limitation of ***a shift register operable to receive the manipulated image data and shift the data into the second memory***. However, Morooka discloses the said limitation.

- Morooka discloses that video random access memory (VRAM) is known as a serial access memory and includes DRAM and a shift register for communicating data to and from DRAM (Col. 7, lines 66-68). Morooka's invention comprises a serial access memory system and apparatus, wherein a shift register shifts video data, which specifically is manipulated image data, from a first memory to a second memory (Col. 8, lines 1-30 and FIG. 1, No. 20, 30, and 40).

15. It would have been obvious to one or ordinary skill in the art to take the teachings of Ceglio et al. and Johnson, and to add from Morooka, the method and apparatus of shift register for receiving the manipulated image data and shifting the data into the second memory. The shift register performs shift operation on the image data according to the internal clock or any other timing mechanism for synchronizing the image data transfer with the projection of the image data onto the subject. In addition, all references are directed, at least in part, to processing and converting image data. Further, Ceglio et al. discloses the limitation of DRAM, which is also disclosed by Morooka. Addition of a shift register to the DRAM will effectively creates VRAM for processing video image data. DRAM used for Video RAM (VRAM) has an additional long shift register that can be loaded from the row buffer. The shift register can be regarded as a second interface to the memory that can be operated in parallel to the normal interface. This is especially useful in frame buffer for CRT displays. These frame buffers generate a serial data stream that is sent to the CRT to modulate the electron beam. By using the shift register in the VRAM to generate this stream, the memory is

available to the computer through the normal interface most of the time for updating the display data, thereby speeding up display data manipulations.

16. Claims 10, 12, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ceglio et al. in view of Johnson as applied to claims 7 and 13 above, and further in view of Nobutani et al., U.S. Patent No., 5,907,329.

17. In regards to claim 10, Ceglio et al. discloses the limitations of a first memory and a second memory as applied to claim 7 above, but does not explicitly disclose the limitation wherein ***the second memory is a frame buffer***. Nobutani et al. discloses the said limitation.

- Nobutani et al. discloses a system and apparatus for processing image data and controlling the display of said processed image data. Said system and apparatus comprises a first memory means for storing original image data; a second memory means for storing data in a display format; converting means for converting the image data stored in the first memory means and transferring the converted image data to the second memory means; and an output means for displaying the converted image data stored in the second memory means (Col. 2, lines 40-63).
- In addition, Nobutani et al. discloses that the data stored in VRAM is processed and stored in ***a frame memory***, which specifically is ***a second memory***. Said frame memory specifically is a frame buffer, and the processed data is stored in the frame buffer as a 4 bit data (Col. 6, lines 1-13; Col. 11, lines 49 – Col. 12, lines 16; and FIG. 2).

18. It would have been obvious to one or ordinary skill in the art to take the teachings of Ceglio et al. and Johnson, and to add from Nobutani et al. the method of using a frame memory as the second memory. When the second memory is a frame memory, the desired frame image can be selected from the frame memory for displaying on the display unit such as a pixel panel before projecting the image onto a subject. In addition, all references are directed, at least in part, to processing and converting image data. Further, a frame buffer stores the image pixel by pixel; used as a temporary storage of data that is waiting to be sent to a device; and used to compensate for differences in the rate of flow of data between components of a computer system.

19. In regards to claim 12, the same basis and rationale for claim rejection as applied to claim 10 are applied. In addition, Celig et al. and Nobutani et al. in combination disclose the limitation of ***a selector operable to select a frame from the frame buffer for transfer to the pixel panel.***

- Nobutani et al. discloses the limitation of a frame memory control circuit (FIG. 3, No. 307), which receives an output instruction from the CPU. The output instruction instructs the frame memory control circuit to select specific lines of data to be transferred to the FLCD, which specifically is the output display device (Col. 10, lines 4-15). Thus, the frame memory control circuit specifically is a ***selector***.

20. It would have been obvious to one or ordinary skill in the art to take the teachings of Celig et al. and Johnson, and to add from Nobutani et al. the method of using a selector to select the desired image frame to be transferred to the output display device.

When the second memory is a frame buffer, the desired frame image can be selected by the selector from the frame buffer for displaying on the display unit such as a pixel panel before projecting the image onto a subject. In addition, all references are directed, at least in part, to processing and converting image data.

21. In regards to claim 18, the same basis and rationale for claim rejection as applied to claim 10 are applied. Nobutani et al. discloses the limitation of storing processed data in the frame buffer, wherein the processed data comprises a predetermined 4 bits as applied to claim 10 above.

22. In regards to claim 19, the same basis and rationale for claim rejection as applied to claim 10 and 18 are applied. As applied to claim 10 above, Nobutani et al. discloses the limitation of generating start address information and storing one address information with one line image data. Thus, an addressed must be generated for each image portion of predetermined number of bits (4 bits).

23. In regards to claim 20, the same basis and rationale for claim rejection as applied to claim 12 and 19 are applied. As applied to claim 10 above, Nobutani et al. discloses the limitation of a first-in, first-out (FIFO) memory capable of storing image data comprising one address information and one line image data. Said FIFO memory has storage capacity large enough to store a plurality of image data portions as applied to claim 10 above. Then the frame memory control circuit selects an image data portion to be transferred to a display unit as applied to claim 12 above.

24. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ceglio et al. in view of Johnson as applied to claims 7 and 13 above, and further in view of Yamada, U.S. Patent No., 5,815,287.

25. In regards to claims 11, Ceglio et al. discloses the limitations of a first memory and a second memory as applied to claim 7 above, but does not explicitly disclose the limitation wherein ***the second memory is a line buffer***. Yamada discloses the said limitation.

- Yamada discloses a image processor comprising a data processing unit (FIG. 1, No. 100) comprising a CPU (FIG. 1, No. 110), a ROM (FIG. 1, No. 120) for storing programs, a DRAM (FIG. 1, No. 130) for temporary storing of original data, a host interface (FIG. 1, No. 140), and a line buffer (FIG. No. 150) (Col. 4, lines 6-15). DRAM specifically is the first memory for storing the image data, and the line buffer is the second memory for storing the manipulated data.

26. It would have been obvious to one or ordinary skill in the art to take the teachings of Celig et al. and Johnson, and to add from Yamada the method of using a line memory as the second memory. When the second memory is a line memory, the desired line of an image can be selected from the lines of images in the line memory for displaying on the display unit such as a pixel panel before projecting the image onto a subject. A line buffer allows sequential transfer of pixels to produce a plurality of lines of output image. Thus, line buffers are useful when only a portion of the image data is

needed to be transferred to be displayed. In addition, both references are directed, at least in part, to processing and converting image data.

27. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ceglio et al. in view of Johnson as applied to claims 7 and 13 above, and further in view of Matsuo et al. as applied to claims 8, 14, and 16 above, and further in view of Nobutani et al. as applied to claims 10 and 12 above.

28. In regards to claim 15, the same basis and rationale for claim rejection as applied to claims 8 and 12 are applied. In order to select a specific frame from the frame memory, the location of said frame must be determined and the frame identified. Calculating the physical memory address of the image frame specifically is determining the location of said frame.

29. It would have been obvious to one of ordinary skill in the art to take the teachings of Ceglio et al., Johnson, and Matsuo et al., and to add from Nobutani et al. the method of frame buffer controller in order to select the desired frame image from the frame buffer for displaying on the display unit. In selecting the desired frame image from the frame buffer, the desired frame image must be identified and the location of the frame image determined. Typically, a buffer will have other attributes such as an input pointer (where new data will be written into the buffer), and output pointer (where the next item will be read from) and/or a count of the space used or free. The input pointer and output pointer specifically identifies frame image in memory and determines the location of said frame image. In addition, there are many different algorithms for using buffers, e.g. first-in first-out (FIFO or shelf), last-in first-out (LIFO or stack), double buffering (allowing one

buffer to be read while the other is being written), cyclic buffer (reading or writing past the end wraps around to the beginning). Thus, in order to execute the FIFO and LIFO algorithms, frame images in memory must be identified and the location determined. Further, all references are directed, at least in part, to processing and converting image data.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hwa C Lee whose telephone number is 703-305-8987. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Mancuso can be reached on 703-305-3885. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hwa C Lee
Examiner
Art Unit 2672

HCL
3/19/04

JOSEPH MANGUSO
PRIMARY EXAMINER